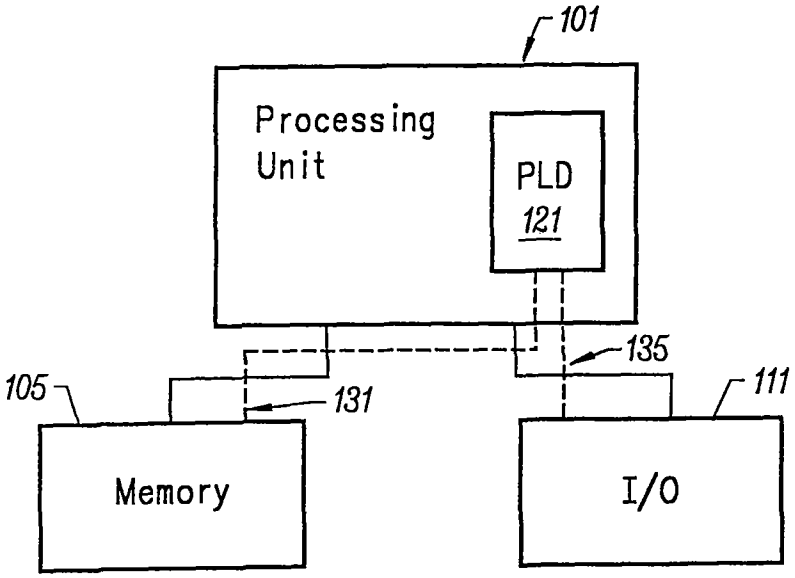


FIGURE 1

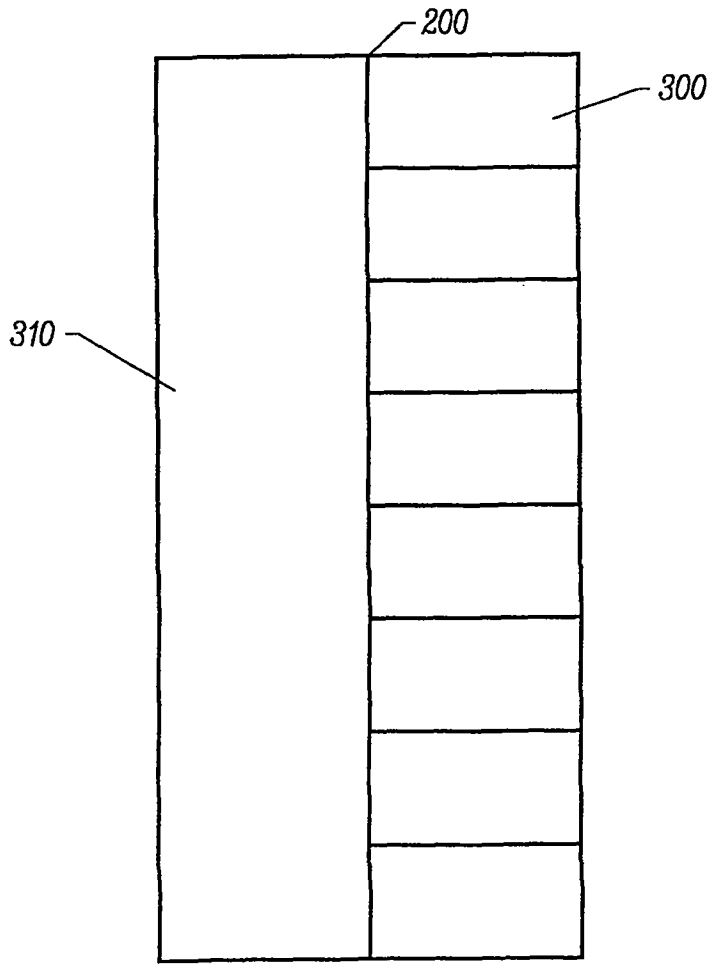


FIGURE 4

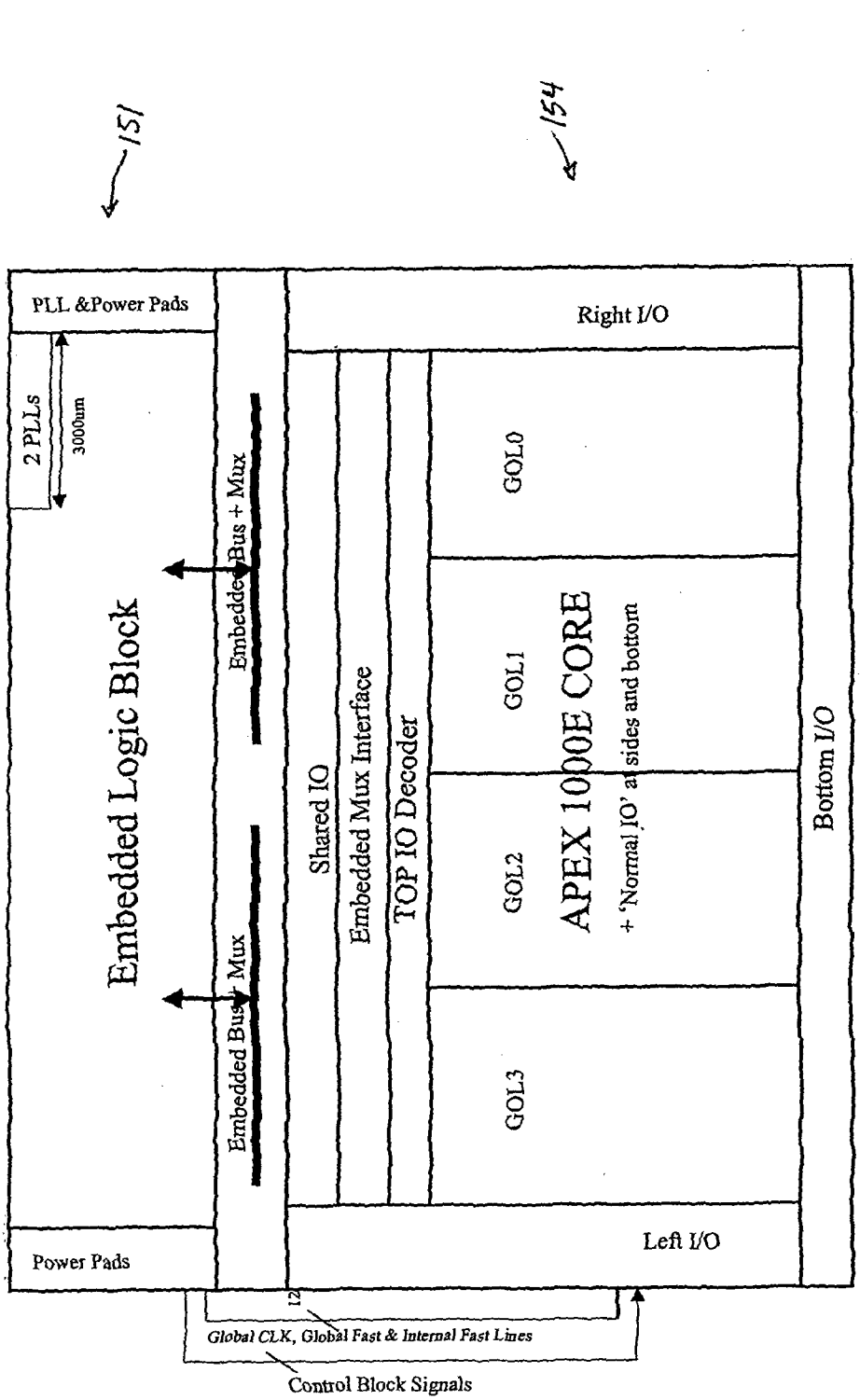

121
151
154
PLL &Power Pads
2 PLLs
3000um
Embedded Logic Block
Embedded Bus + Mux
Embedded Bus + Mux
Power Pads
Shared IO
Embedded Mux Interface
TOP IO Decoder
Right I/O
GOL0
GOL1
GOL2
GOL3
APEX 1000E CORE
+ 'Normal IO' at sides and bottom
Left I/O
Bottom I/O
12
Global CLK, Global Fast & Internal Fast Lines
Control Block Signals
Top Level Floorplan

FIGURE 2

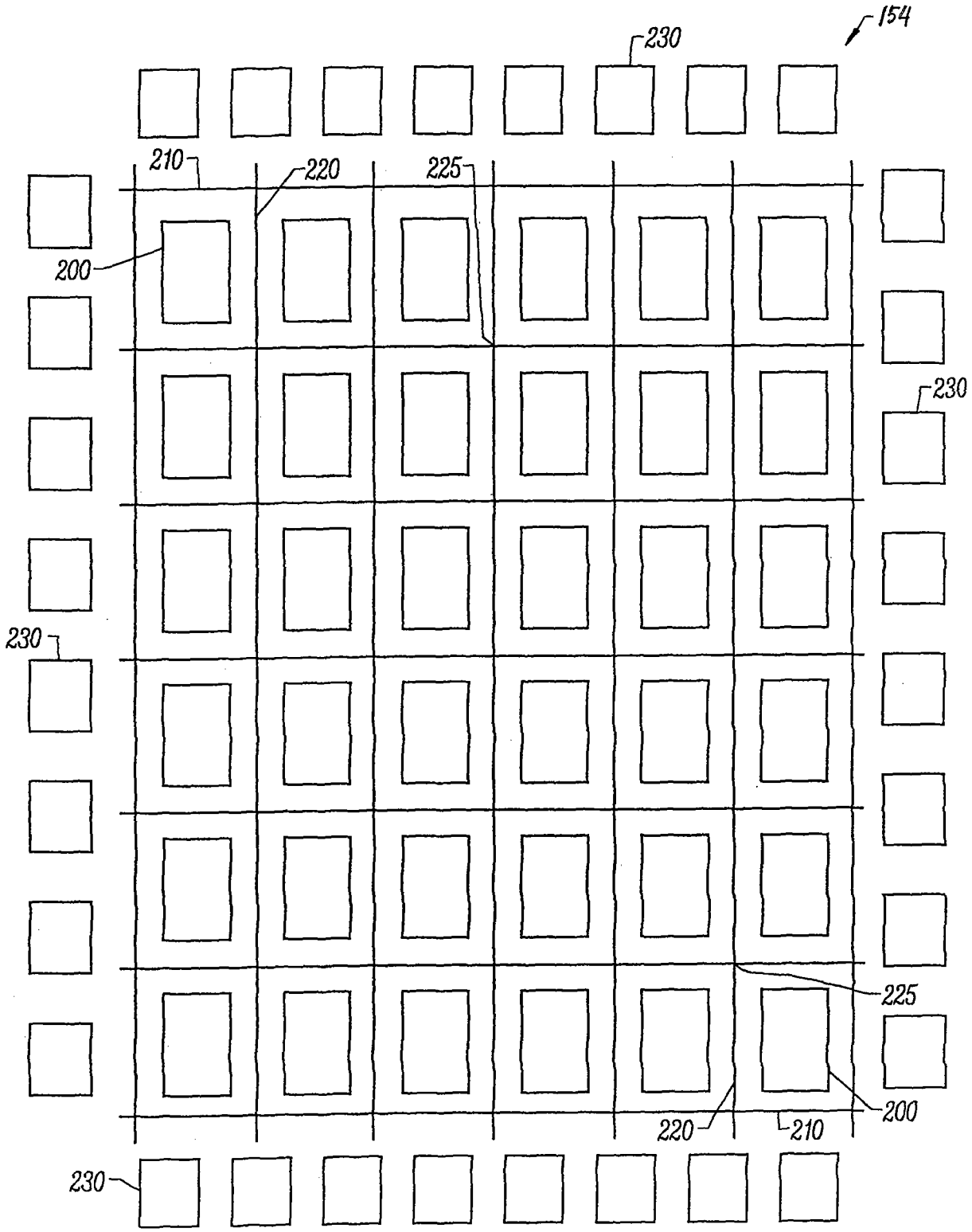


FIGURE 3

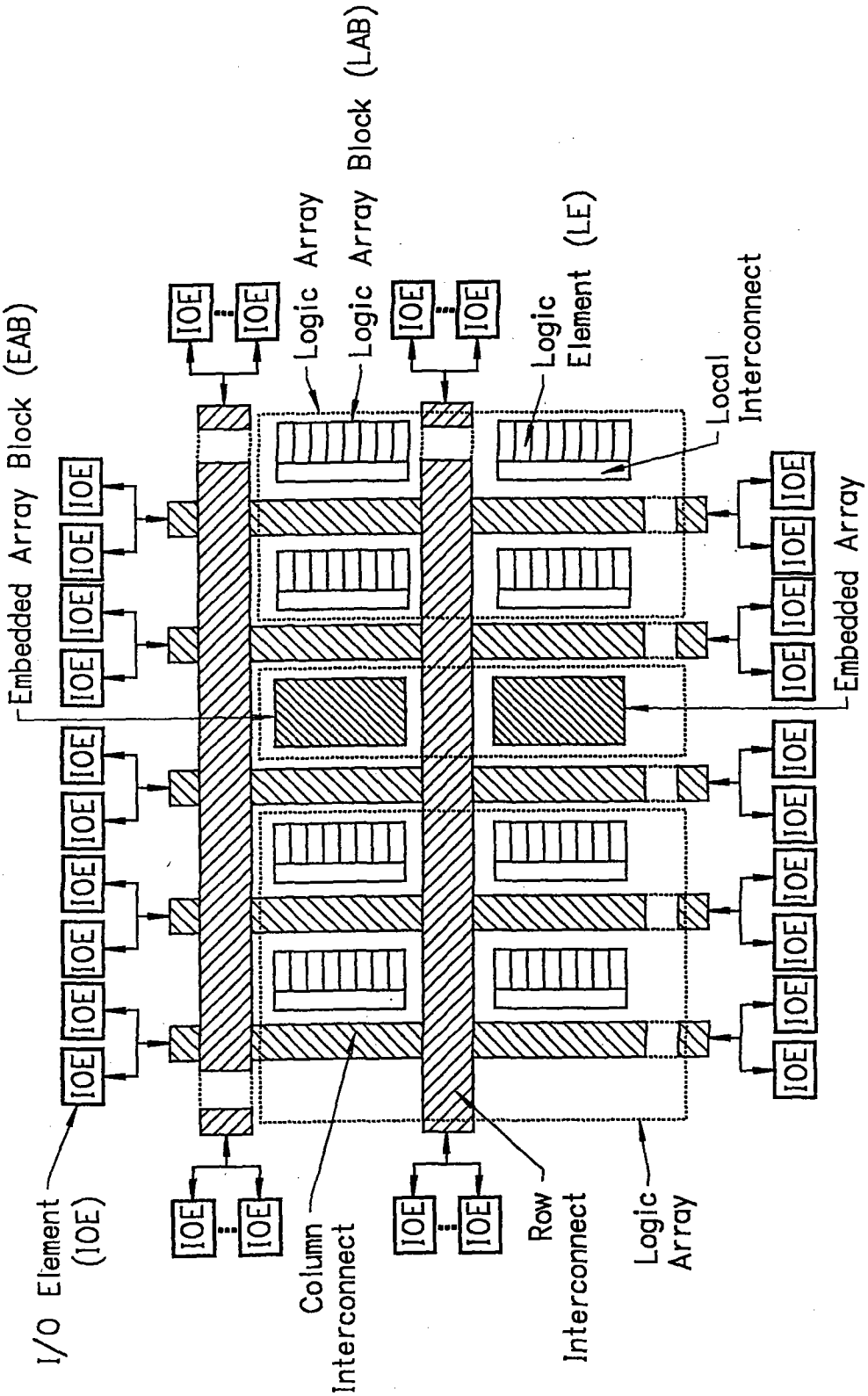

Embedded Array Block (EAB)
Logic Array
Logic Array Block (LAB)
Logic Element (LE)
Local Interconnect
Embedded Array
I/O Element (IOE)
Column Interconnect
Row Interconnect
Logic Array
IOE

FIGURE 5

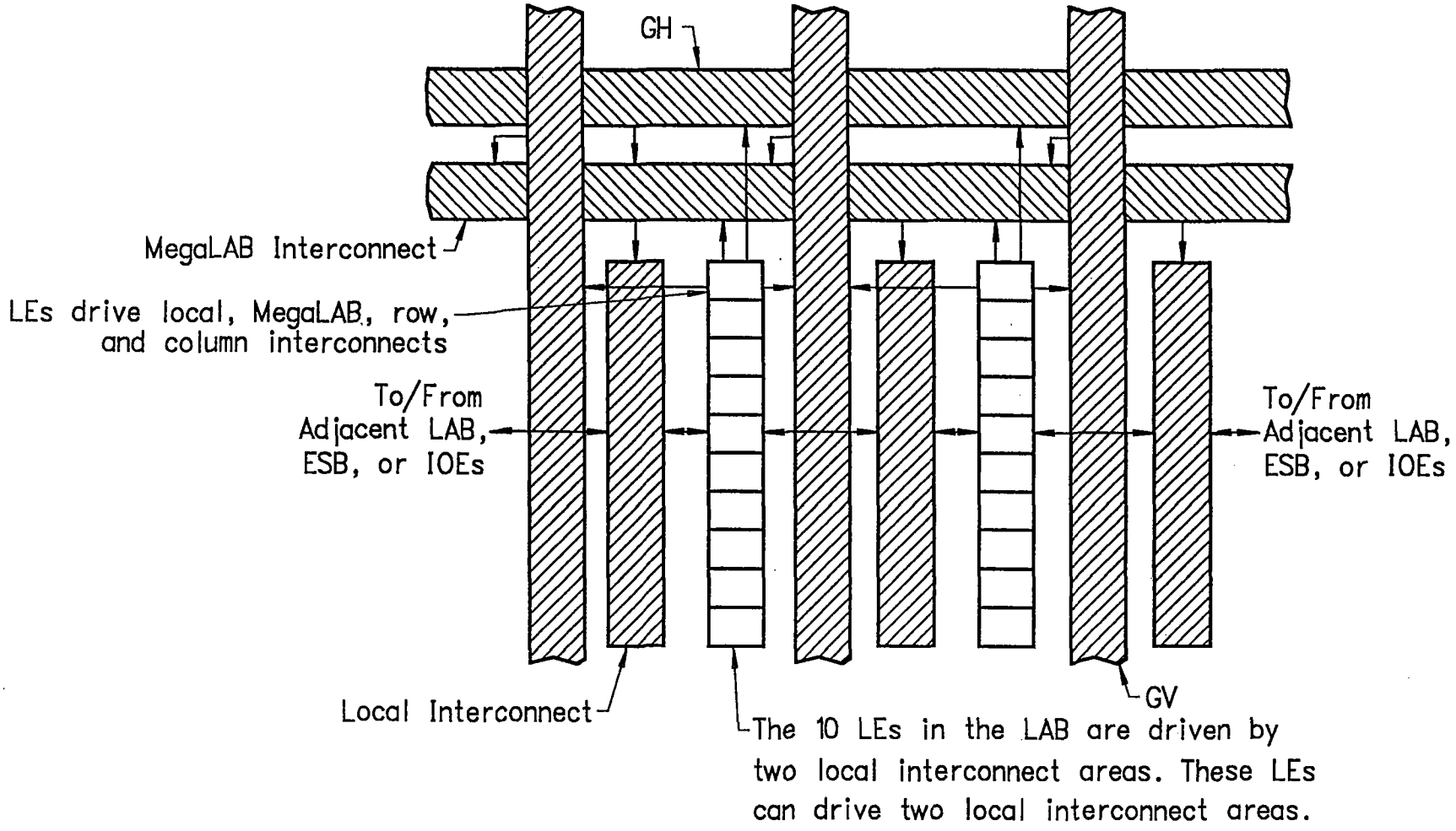

GH
MegaLAB Interconnect
LEs drive local, MegaLAB, row, and column interconnects
To/From Adjacent LAB, ESB, or IOEs
To/From Adjacent LAB, ESB, or IOEs
Local Interconnect
GV
The 10 LEs in the LAB are driven by two local interconnect areas. These LEs can drive two local interconnect areas.

FIGURE 6

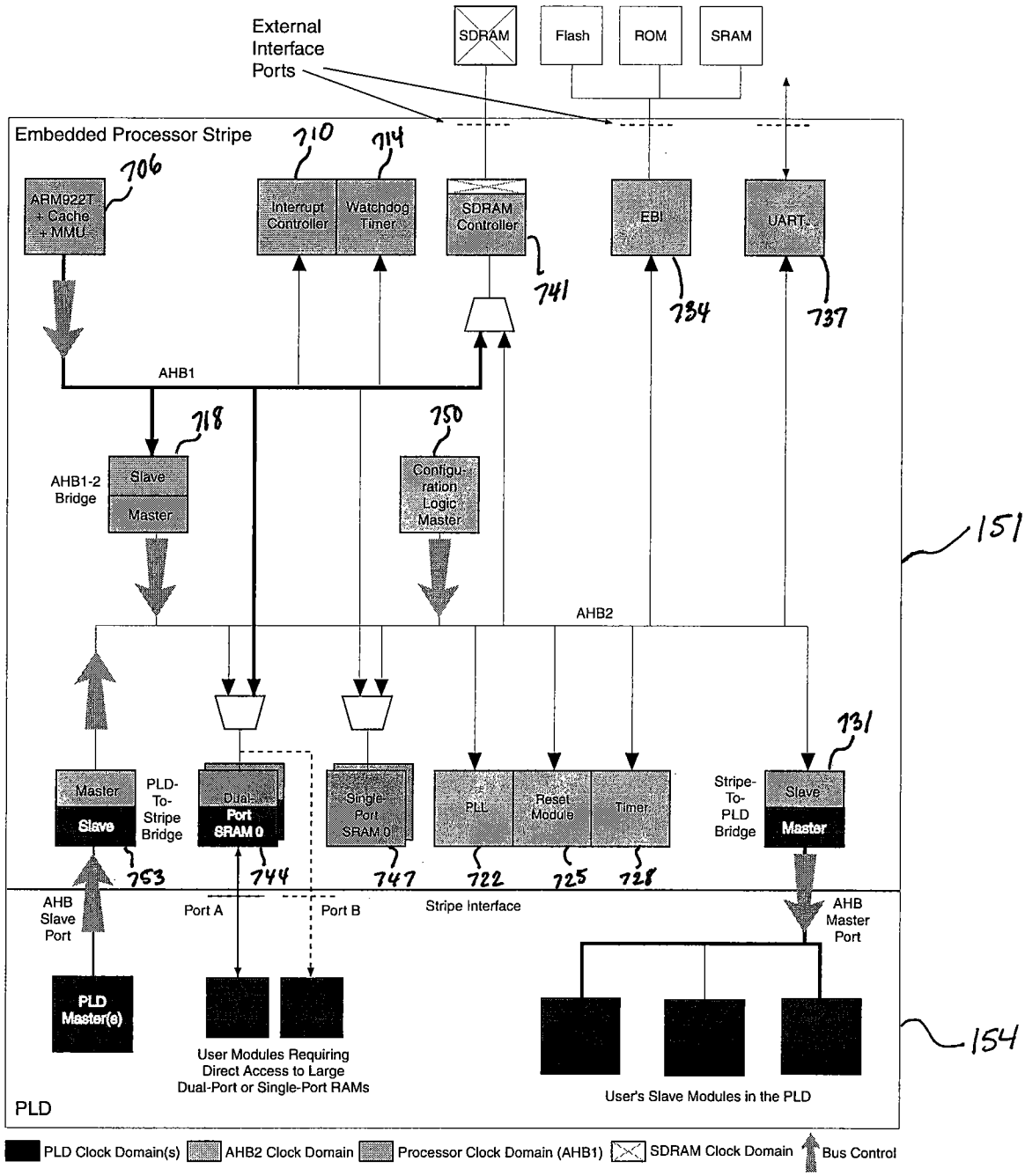

External Interface Ports
SDRAM
Flash
ROM
SRAM
Embedded Processor Stripe
710
714
706
ARM922T + Cache + MMU
Interrupt Controller
Watchdog Timer
SDRAM Controller
EBI
UART
741
734
737
AHB1
718
750
AHB1-2 Bridge
Slave
Master
Configu-ration Logic Master
151
AHB2
731
Master
Slave
PLD-To-Stripe Bridge
Dual-Port SRAM 0
Single-Port SRAM 0
PLL
Reset Module
Timer
Stripe-To-PLD Bridge
Slave
Master
753
744
747
722
725
728
AHB Slave Port
Port A
Port B
Stripe Interface
AHB Master Port
PLD Master(s)
User Modules Requiring Direct Access to Large Dual-Port or Single-Port RAMs
User's Slave Modules in the PLD
154
PLD
PLD Clock Domain(s)
AHB2 Clock Domain
Processor Clock Domain (AHB1)
SDRAM Clock Domain
Bus Control

FIGURE 7

FIGURE 8

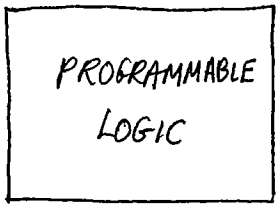


FIGURE 9

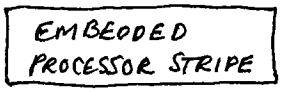


FIGURE 10

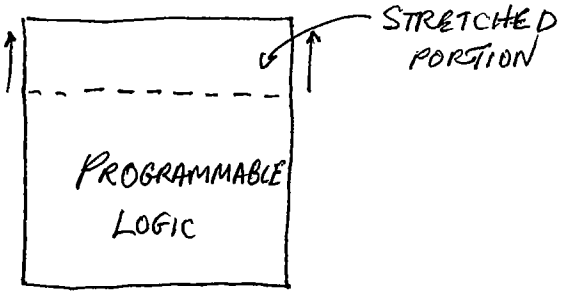
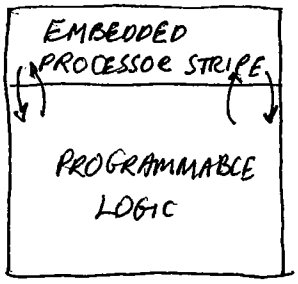


FIGURE 11



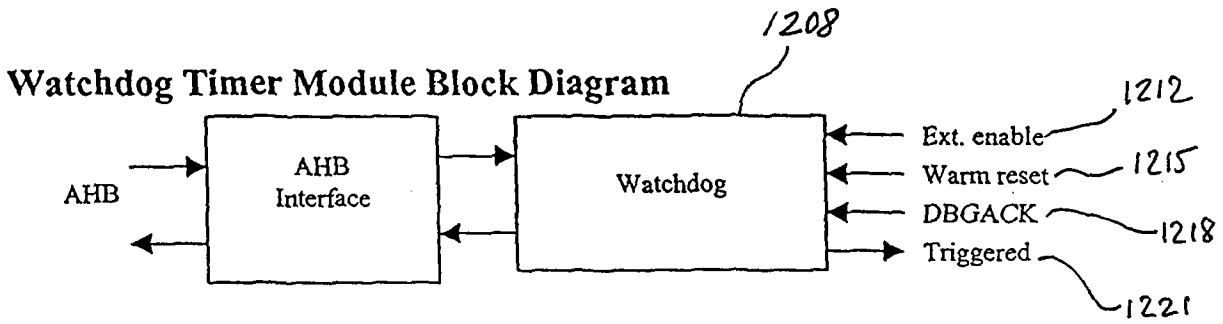


FIGURE 12

Control Register (WDOG_CR) – Read/Write

Register : WDOG_CR Address : Address Base + 0x4C0 Access: Read/Write

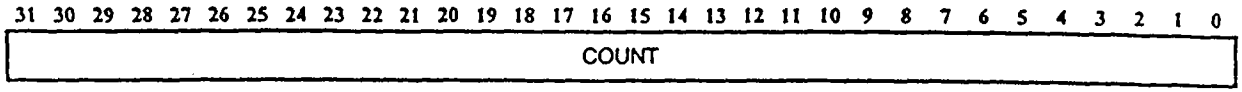
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																												TRIGGER												0			LK

LK	R/W	When this bit has the value 1 further writes to the register have no effect.
TRIGGER	R/W	0 means watchdog disabled. Other values specify bits 29:4 of the trigger value (bits 3:0 of the trigger are always zero.
0	R	Reserved for future use. Write as 0 to ensure future compatibility.

FIGURE 13

Count Register (WDOG_COUNT) – Read Only

Register : WDOG_COUNT Address : Address Base + 0x4C4 Access: Read

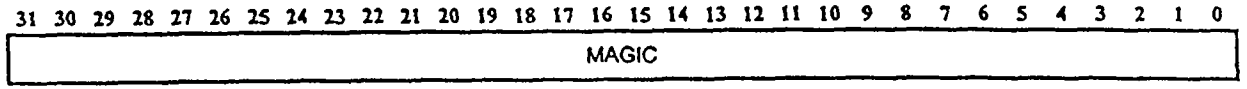


COUNT	R	Current value of watchdog count register.

FIGURE 14

Reload Register (WDOG_RELOAD) – Write Only

Register : WDOG_RELOAD Address : Address Base + 0x4C8 Access: Write



MAGIC	W	Magic value to reset watchdog.

FIGURE 15

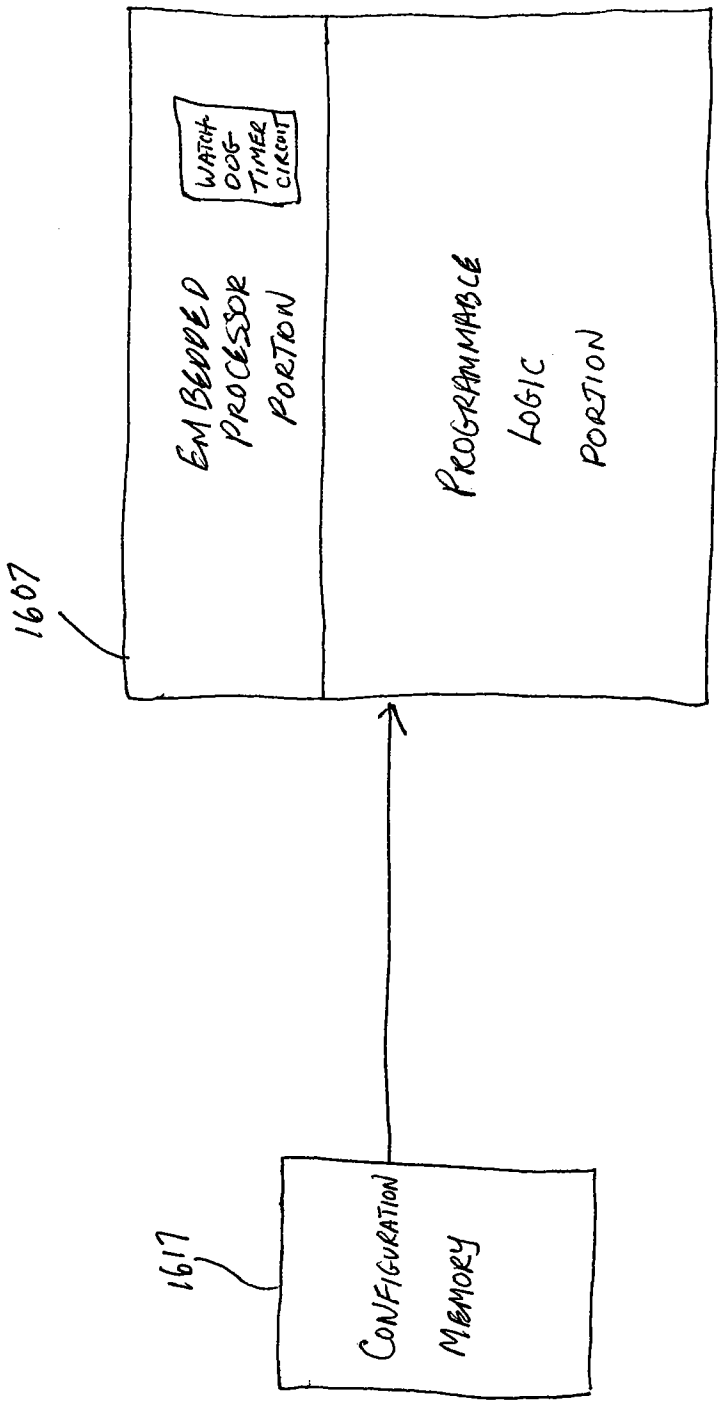

1607
EMBEDDED PROCESSOR PORTION
WATCH-DOG-TIMER CIRCUIT
PROGRAMMABLE LOGIC PORTION
1617
CONFIGURATION MEMORY

FIGURE 16

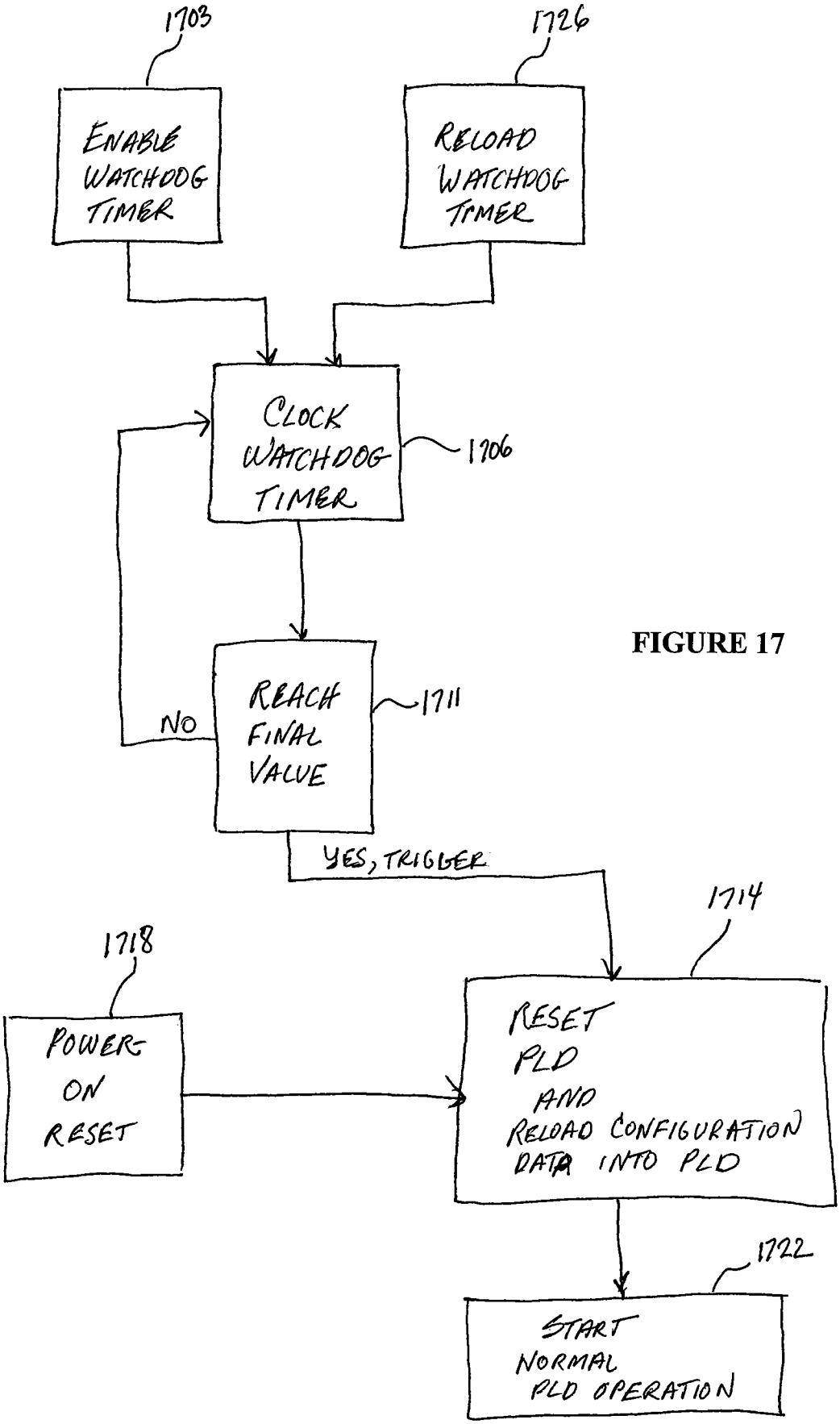

1703
1726
ENABLE WATCHDOG TIMER
RELOAD WATCHDOG TIMER
CLOCK WATCHDOG TIMER
1706
REACH FINAL VALUE
1711
NO
YES, TRIGGER
1714
1718
POWER-ON RESET
RESET PLD AND RELOAD CONFIGURATION DATA INTO PLD
1722
START NORMAL PLD OPERATION

FIGURE 17